Example 1: Design a modulo-8 binary-up counter using T- Flip Flop

- ✓ Modulo 8 counter : Counts upto 7. So we need three Flip-flops for eight states

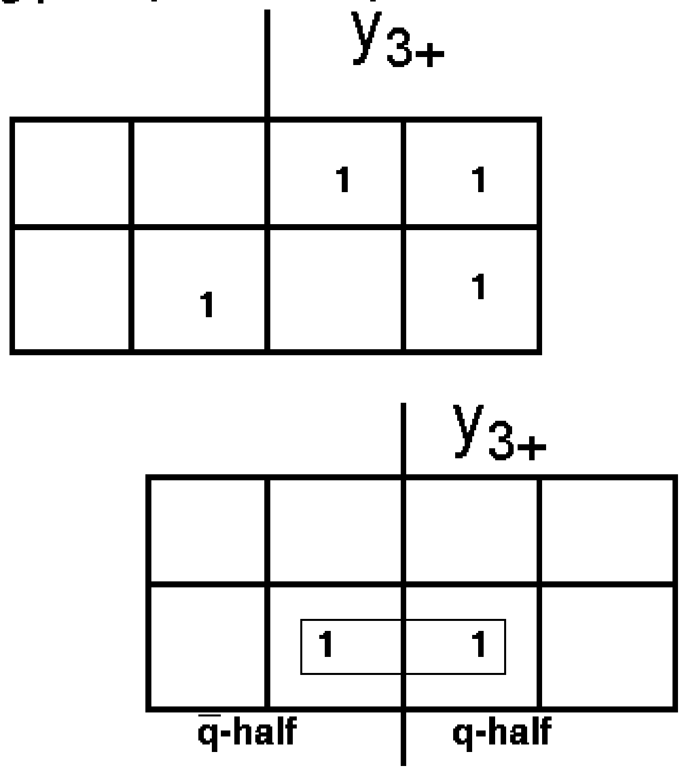
Truth Table

y_3	y_2	y_1	y_{3+}	y_{2+}	y_{1+}	z
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	1	0	1	0
1	0	1	1	1	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	1

" Z " is the output

Modulo-8 counter

$y_{3+} = \Sigma(3,4,5,6)$



$T_{y3} = y_1 y_2$

Modulo-8 counter

$y_{2+} = \Sigma(1,2,5,6)$

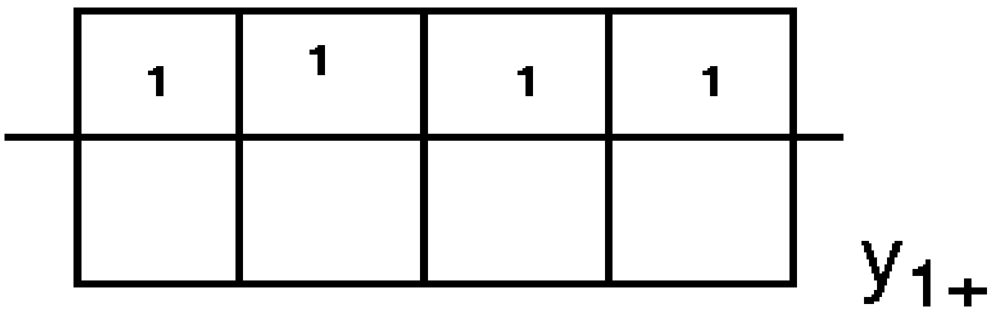
	y_{2+}	y_{2+}	
	1	1	
1			1

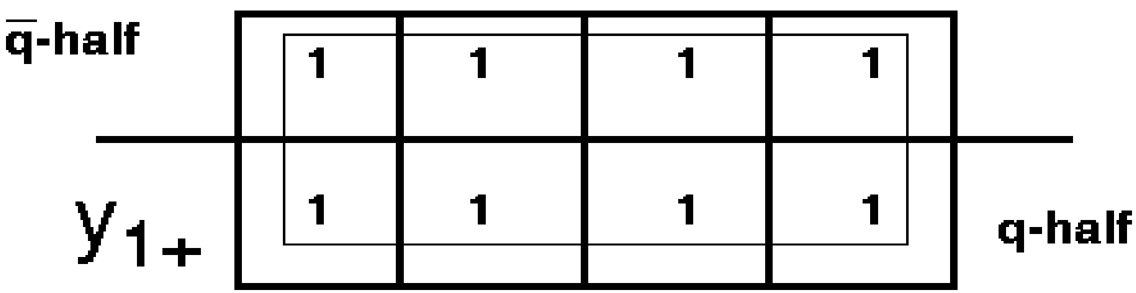
	y_{2+}	y_{2+}	
1	1	1	1
$\bar{q}$-half	q-half	q-half	$\bar{q}$-half

$T_{y2} = y_1$

Modulo-8 counter

$$y_{1+} = \Sigma(0,2,4,6)$$





$$T_{y1} = 1$$

Example 2:Design a modulo-8 binary-up counter with input x using T- Flip Flop

- ✓ Modulo 8 counter : Counts upto 7 . So we need three Flip-flops for eight states

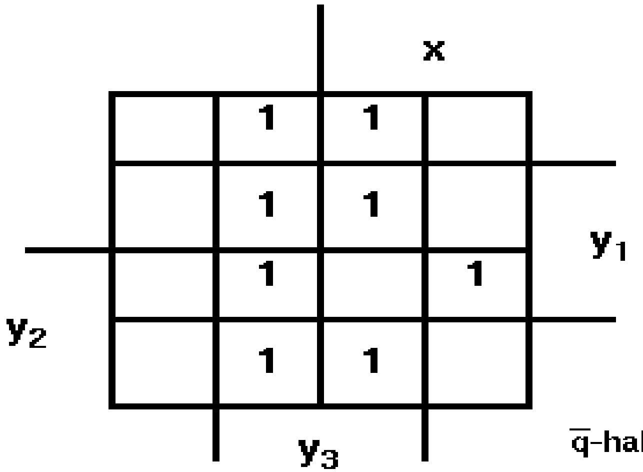
x	y_3	y_2	y_1	y_{3+}	y_{2+}	y_{1+}
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	1
1	0	1	1	1	0	0
1	1	0	0	1	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1
1	1	1	1	0	0	0

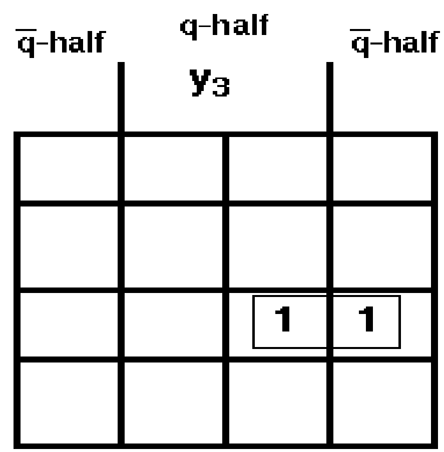
$$y_{3+} = \Sigma(4,5,6,7,11,12,13,14)$$

$$y_{2+} = \Sigma(2,3,6,7,9,10,13,14)$$

$$y_{1+} = \Sigma(1,3,5,7,8,10,12,14)$$

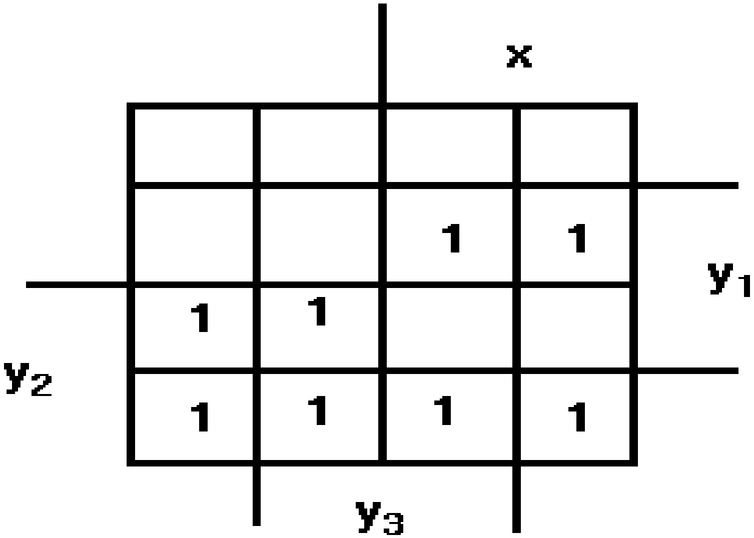
Example 2: modulo 8 counter with I/p x



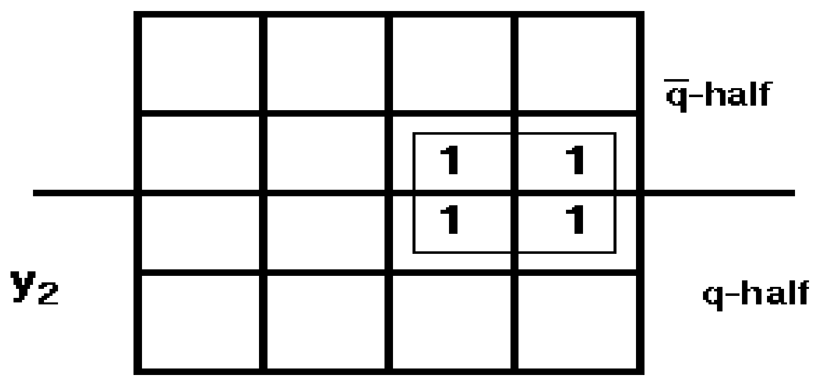


$T_{y3} = xy_1y_2$

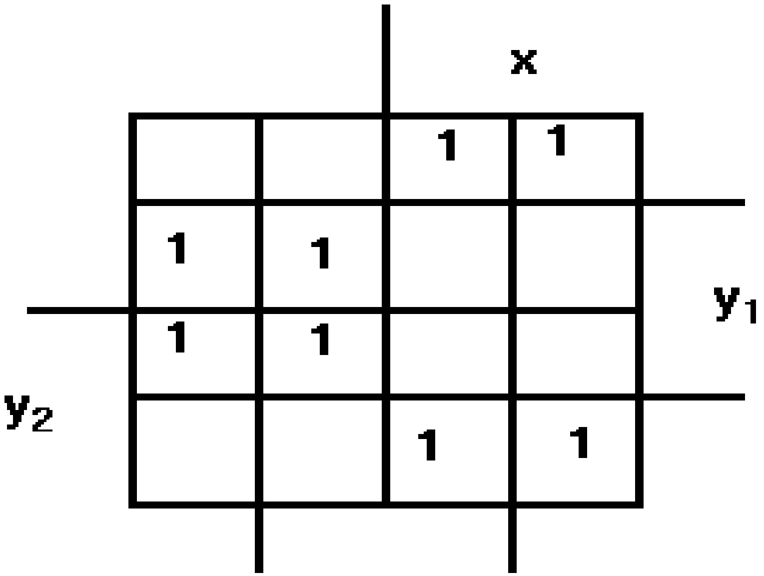
Example 2: modulo 8 counter with I/p x



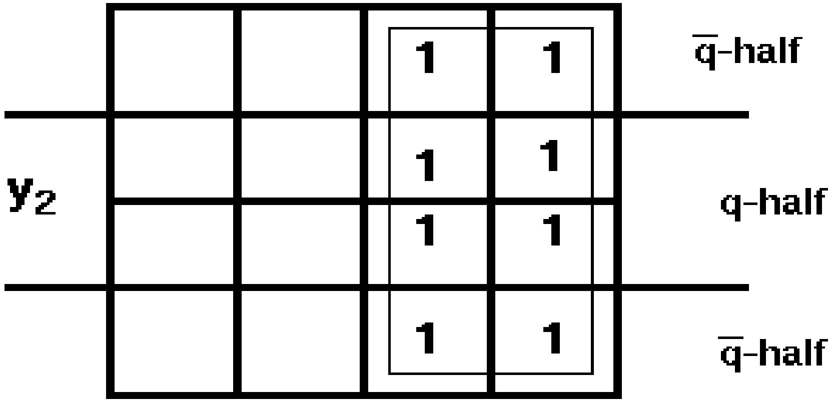
$$T_{y2} = xy_1$$



Example 2: modulo 8 counter with I/p x



$$T_{y1} = X$$



Example 3: Design a binary-down decade counter using SR- Flip Flop without input x

- ✓ Decade Counter: Counts up to 9 . So we need four Flip-Flops for ten states

y_4	y_3	y_2	y_1	y_{4+}	y_{3+}	y_{2+}	y_{1+}
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	1	1	1
1	0	0	1	1	0	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

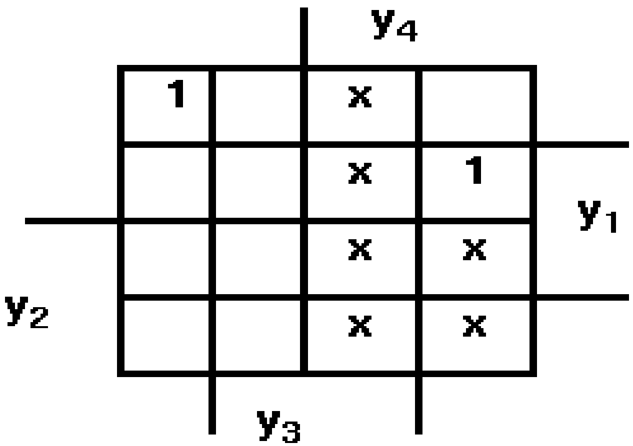
$$y_{4+}=\Sigma(0,9)+\Sigma_x(10,11,12,13,14,15)$$

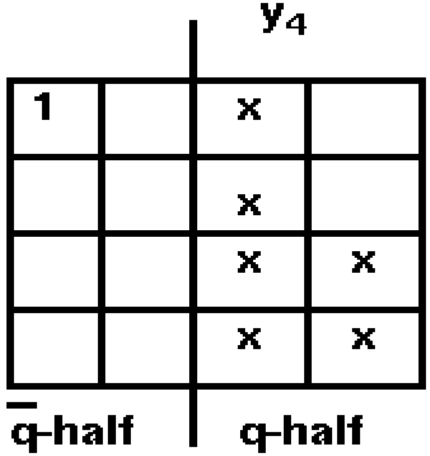
$$y_{3+}=\Sigma(5,6,7,8)+\Sigma_x(10,11,12,13,14,15)$$

$$y_{2+}=\Sigma(3,4,7,8)+\Sigma_x(10,11,12,13,14,15)$$

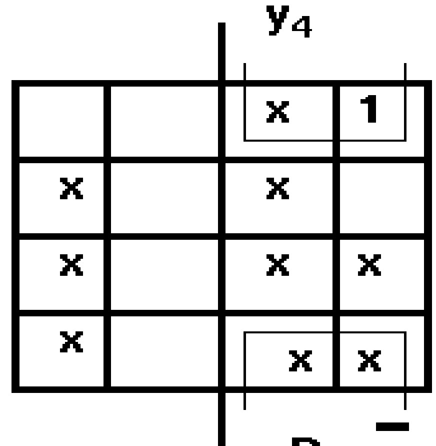
$$y_{1+}=\Sigma(0,2,4,6,8)+\Sigma_x(10,11,12,13,14,15)$$

Example 3: Binary decade counter



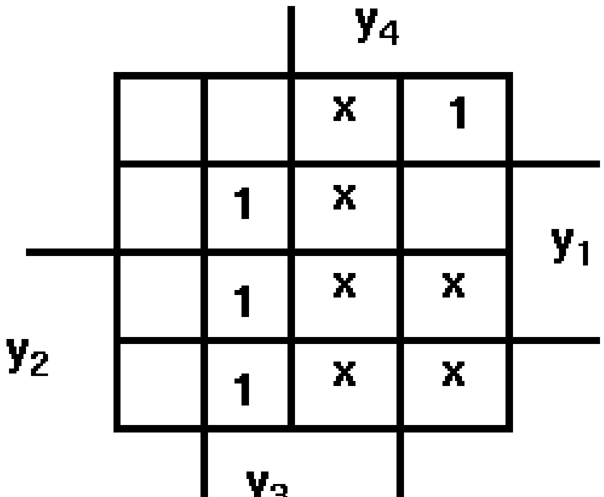


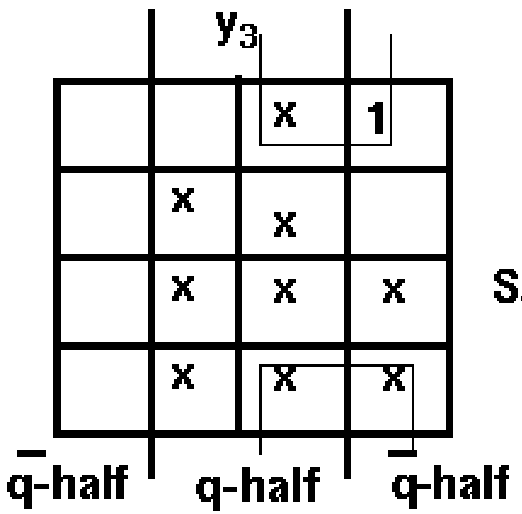
$S_{y4} = \bar{y}_1 \bar{y}_2 \bar{y}_3 \bar{y}_4$



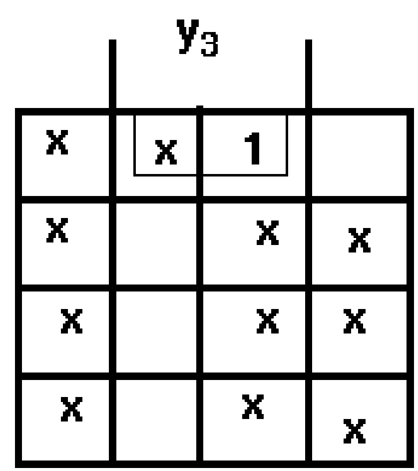
$R_{y4} = \bar{y}_1 y_4$

Example 3: Binary decade counter



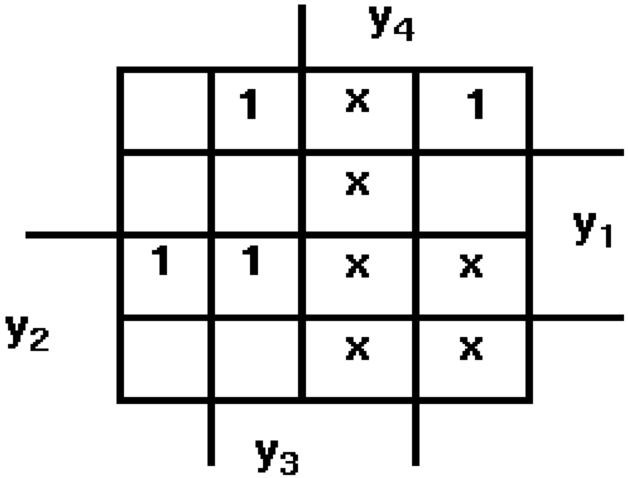


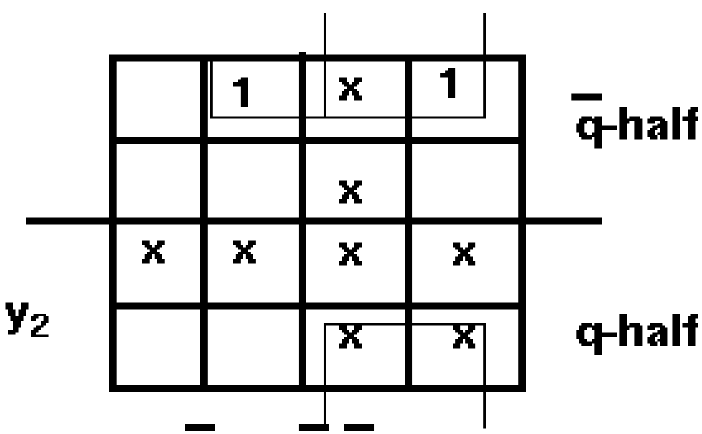
$S_{y3}=\bar{y}_1 y_4$



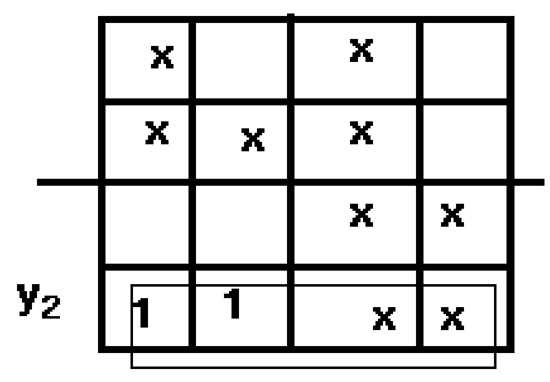
$R_{y3}=\bar{y}_1\bar{y}_2 y_3$

Example 3: Binary decade counter



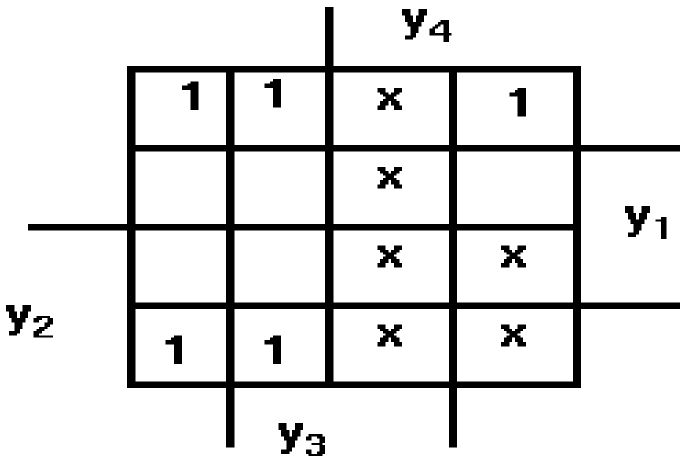


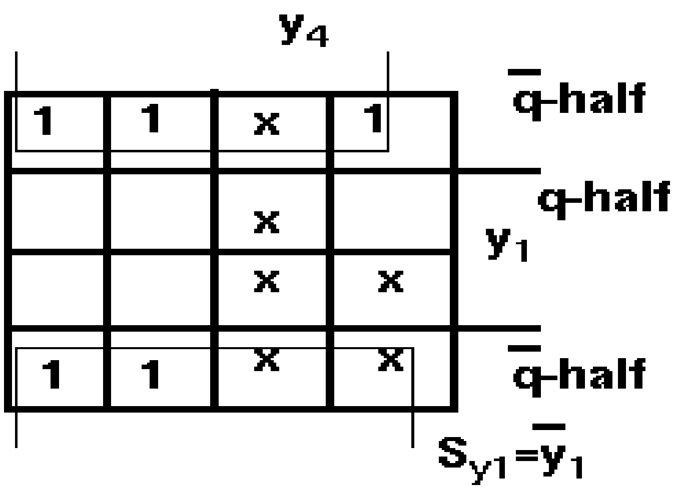
$S_{y2} = \bar{y}_1 y_4 + \bar{y}_1 \bar{y}_2 y_3$

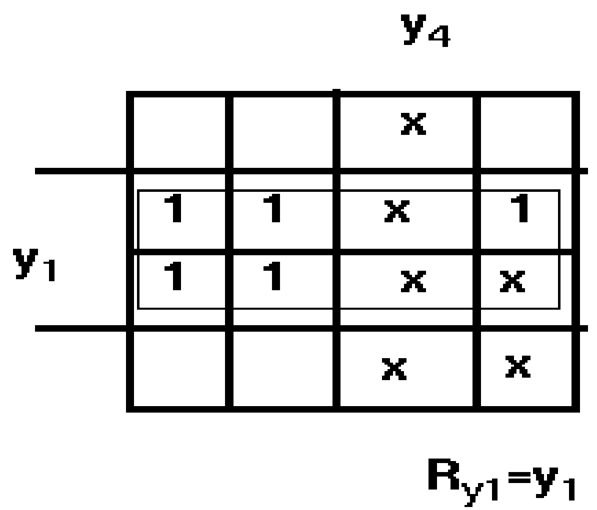


$R_{y2} = \bar{y}_1 y_2$

Example 3: Binary decade counter

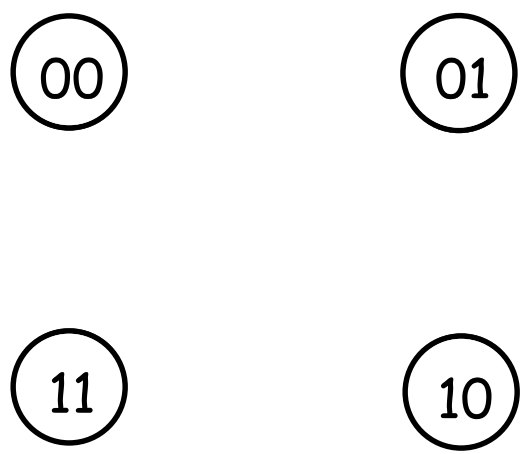






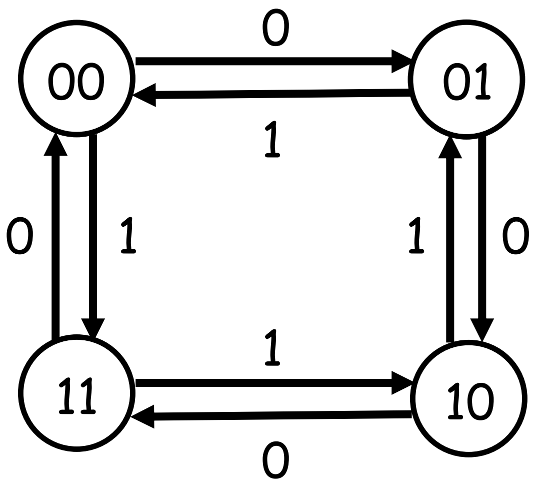
A slightly fancier counter

- Let's try to design a slightly different two-bit counter:
  - Again, the counter outputs will be 00, 01, 10 and 11.
  - Now, there is a single input, X. When X=0, the counter value should *increment* on each clock cycle. But when X=1, the value should *decrement* on successive cycles.
- We'll need two flip-flops again. Here are the four possible states:



The complete state diagram and table

- Here's the complete state diagram and state table for this circuit.



Present State Q_1	Q_0	Inputs X	Next State Q_1	Q_0
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

D flip-flop inputs

- ✓ If we use D flip-flops, then the D inputs will just be the same as the desired next states.
- ✓ Equations for the D flip-flop inputs are shown at the right.
- ✓ Why does $D_0 = Q_0'$ make sense?

Present State Q_1	Present State Q_0	Inputs X	Next State Q_1	Next State Q_0
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

			Q_0	Q_0
	0	1	0	1
Q_1	1	0	1	0
		X	X	

$$D_1 = Q_1 \oplus Q_0 \oplus X$$

			Q_0	Q_0
	1	1	0	0
Q_1	1	1	0	0
		X	X	

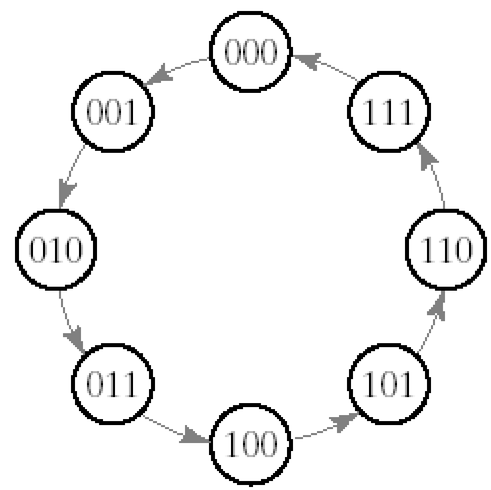
$$D_0 = Q_0'$$

Example 5: Synthesis Using T Flip-Flops

✓ The synthesis using T flip-flops will be demonstrated by designing a binary counter. An n-bit binary counter consists of n flip-flops that can count in binary from 0 to 2^n-1. The state diagram of a 3-bit counter is:

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) T

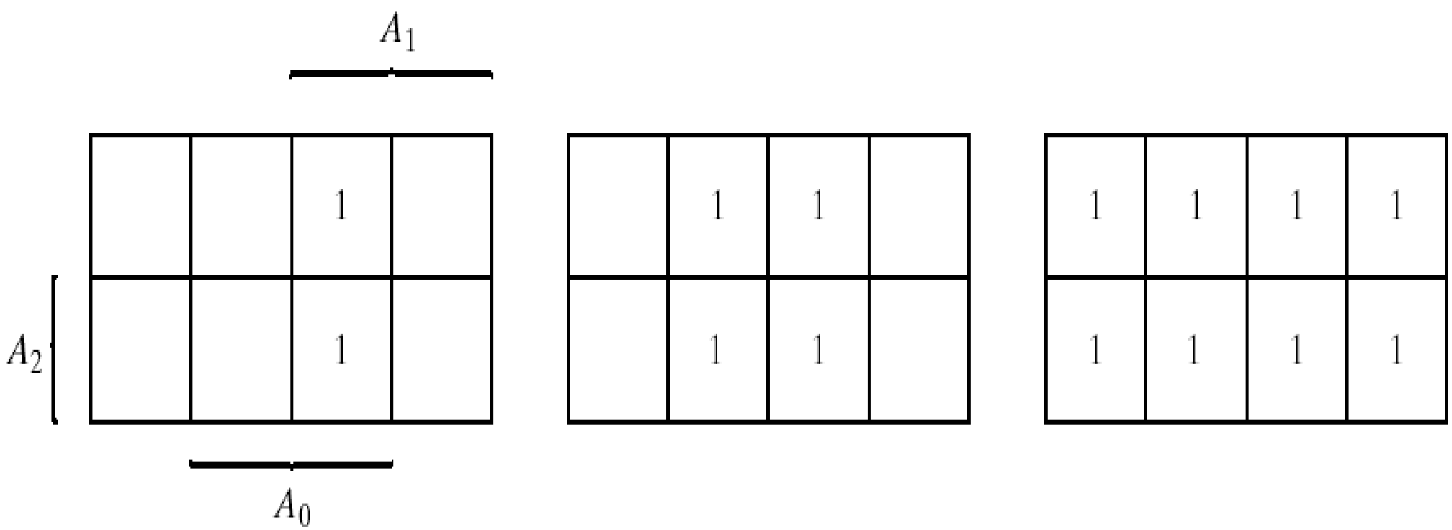


Synthesis Using T Flip-Flops

Table 5-14
State Table for 3-Bit Counter

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

Synthesis using T Flip-Flops



$T_{A2} = A_1 A_0$ $\qquad$ $T_{A1} = A_0$ $\qquad$ $T_{A0} = 1$

Table 5-14
State Table for 3-Bit Counter

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

Synthesis Using T Flip-Flops